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Complete if Known

Application Number	09/471,877
Filing Date	December 23, 1999
First Named Inventor	Adrian Sfarti
Art Unit	2183
Examiner Name	Daniel H. Pan
Attorney Docket Number	0100.9910145

Sheet 1 of 1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
		CARROLL, MARK et al.; Intel ties upcoming PC-on-a-chip to Rambus; EE Times Online; from www.eet.com; May 28, 1999; pages 1-5.	
		WADE, WILL; Intel delays Timna after finding glitch in Rambus component; EE Times Online; from www.eet.com; June 6, 2000; pages 1-3.	
		LAMMERS, DAVID; Intel drops Timna integrated CPU project; EE Times Online; from www.eet.com; September 29, 2000; pages 1-4.	

Examiner Signature	Date Considered
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached to process an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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